REMARKS:

The Examiner is thanked for his courtesy in discussing the outstanding Office Action on February 19, 2002 and the grounds of rejection under 35 US 103 will be addressed on the basis set forth in the Interview Summary mailed February 27, 2002.

Claim Rejections - 35 US 112

Claims 66-74 have been rejected under 35 US 112, first paragraph. In the Official Action, it is asserted: *"Application S.N. 08/586,411 fails to describe the process of example B in figure 4 of Ference with sufficient specificity to warrant a conclusion that the composition of deuterium in the gate oxide that is described by Ference is an inherent property of Applicant's written description."* To support this assertion, the Examiner references Applicant's specification at pages 10-11 of application 08/586,411 ('411 application)and then asserts: *"Applicant must show that the claimed concentration necessarily results from what is described in application S. N. 08/586,411 and is not just a possible outcome that is achieved by picking and choosing certain processes from the disclosed list of process alternatives in the application."* The Examiner is respectfully referred to the description at page 14-18 of the '411 application, identified in the tabulation of supporting disclosure for claim 66 in the tabulation on page 5 of the "Request by Applicant for Interference With Patent under 37 CFR 1.607" mailed February 8, 2001.

Page 14, lines 5, *et seq.* of the '411 application includes the description: *"The wafers used in these examples contained NMOS transistor structures fabricated using AT&T's 0.5mm 3.3 volt CMOS technology generally as described in I.C. Kizilyalli and M. J. Thoma, et al., IEEE Trans. Semiconductor Manufacturing 8, 440 (1995), (IEEE publication) with the following changes"* (the changes relate to gate oxide thickness, p-well doping, and LDD region implant) and the publication is incorporated by reference into the '411 application (see '411 application page 18, lines 16-20). A copy of the IEEE publication is provided for the convenience of the Examiner. Page 441 , right column, of the IEEE publication describes " *Heavily doped N+ polysilicon (2500A) serves as a gate electrode."* The wafers

thus fabricated were subsequently subjected to Deuterium annealing as described at pages 15-18. Consequently, the '411 application does disclose that Deuterium annealing takes place after at least gate contact formation.

Withdrawal of this ground of rejection of claims 66-74 under 35 US 112 is respectfully requested.

The grounds of rejection of claims 67-69 and 72 under 35 US 112 is believed to be moot following amendments to claims 67, 69 and 72 presented herein and withdrawal of these grounds rejections of claims 67-72 is respectfully requested.

It is believed that all of claims 66-74 comply with 35 US 112.

Rejection under 35 US 103

In the Examiner's communication mailed 02/27/2002, it has been clarified that Claims 40-48, 60-65, and 75-78 have been rejected under 35 USC 103 as unpatentable over US Patent 5,514,628 ("Enomoto") in view of PCT International Application WO 94/19829 ("Lisenker").

In the Office action mailed December 20, 2001, the Examiner concedes *". . . Lisenker alone does not teach a deuterium annealing step that occurs after electrical contacts have been formed over a semiconductor device."* After a discussion of both references, the Examiner asserts: *"It would have been obvious to one of ordinary skill in the art at the time of the invention to replace the hydrogen of the post metallization anneal step in Enomoto, with deuterium, as suggested by Lisenker."* This rejection is respectfully traversed.

Enomoto is directed to *"a technique for improving yield with the use of cell replacement through redundancy"* (Abstract). Enomoto discloses in relation to DRAM manufacture, exemplified by a 64 million cell device: *"In order to increase yield in semiconductor memories, redundant structures are provided on the device allowing replacement of defective*

portions of the device."(co. 1, lines 33-35.) Further, Enomoto states: *"One problem that has occurred as the density of the memory arrays have increased is failures that occur after the cell replacement and subsequent burn-in. . . . One failure mechanism is high leakage current due to interface trap density. In order to lower the interface trap density and stabilize the operation of the device, the device is subjected to an annealing process (hereinafter referred to as "sinter"). . . . One problem that exists with this procedure is that, in certain marginal cells, the hydrogen termination that is provided during the sintering operation is broken during the reliability test. . . . This results in increased leakage current at a higher level than the specified level."*(col. 1, line 45 – col. 2, line 11.)

Enomoto proposes a solution to this problem by a process which *". . . includes the first step of subjecting the integrated circuit to an insufficient sinter operation. This is performed after formation of the circuitry on the integrated circuit. The insufficient sinter operation is performed at a temperature that will not cause a substantial decrease in the interface trap density in the integrated circuit. Thereafter, the integrated circuit is tested to determine if any of the circuitry on the integrated circuit corresponding to the redundant circuitry is defective. If defective, the defective circuitry is replaced with the corresponding redundant circuitry. Thereafter, the integrated circuit is subjected to a sufficient sinter operation for a predetermined amount of time. The sufficient sinter operation is carried out at a temperature that will substantially decrease the interface trap density. Thereafter, the integrated circuit is subjected to a reliability and burn-in test procedure."*(col. 2, lines 3-22.)

In contrast, Lisenker's teaching is directed to reducing the effects of electrical stress caused by "hot" electrons (carriers) in a semiconductor device by annealing in a deuterium containing atmosphere, see, for example, page 3, line 31 – page 5, line 5. The Examiner recognizes " . . . Lisenker alone does not teach a deuterium annealing step that occurs after electrical contacts have been formed over a semiconductor device."

Consequently, neither Lisenker nor Enomoto suggest the employment of Lisenker's annealing process in Enomoto's manufacturing operations on completed integrated

circuit structures. This conclusion is reinforced by the different problems addressed by Lisenker and Enomoto. Lisenker's concerns address annealing during device processing to reduce device degradation due to "hot" carrier stress during operation. Enomoto, is directed, not to reduction of the effects of "hot" carrier stress during memory array operation (which at early 1996 were not an issue in DRAM operation) but to elimination of defective cells in the memory array before completion of manufacture, i.e. before the device is placed into operation.

In addition, claim 40 is further distinguished from Lisenker and Enomoto by the lifetime improvement characteristics recited in the final clause of claim 40 which constitute a measurable, structural characteristic (see page 22, line 14 to page 23, line 3 of Applicants' specification) of the device set forth in that claim. Similar comment are applicable to claims 62, 75 and 76.

For the reasons set forth above, it is believed claims 40-48, 60-65 and 75-78 are not rendered unpatentable by Enomoto and Lisenker. Favorable reconsideration is respectfully requested.

New claims 79-81 are patentably distinguished from Enomoto and Lisenker for the reasons advanced with respect to claims 40, 75 and 76, respectively and in addition because of the feature *"the gate insulating layer having a thickness not exceeding about 55 Angstroms"* as recited in claim 79 with similar recitations in Claims 80 and 81. This feature is not disclosed or suggested by either Lisenker or Enomoto and is advantageous in achieving the beneficial characteristics of improved resilience to hot carrier stress characterizing devices as recited in those claims. The Examiner is referred to Applicants' specification at page 18, lines 20-21. Claims 79-81 are believed to be in condition for allowance.

CONCLUSION:

It is believed this amendment and the accompanying remarks have addressed and overcome all outstanding grounds of rejection, demonstrated that the claimed invention is patentable over the references of record, and that all of claims 40-48, 60-65 and 75-78, as well as newly introduced claims 79-81, are in condition for allowance. Early action to that effect will be appreciated.

If after consideration, the Examiner believes that further prosecution of the application may be facilitated by discussion, a telephone call to the undersigned attorney at 972-702-7940 will be appreciated.

Attached hereto is a marked up version of the changes made to the specification and claims by the current amendment. The attached page is captioned **"Version with markings to show changes made."**

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the claims:

The following claims have been amended as shown:

40. (Twice Amended) A semiconductor device comprising a field effect transistor having an interface between a semiconductive silicon layer and a gate ~~oxide~~ insulating layer, structurally characterized by the presence of deuterium at said interface resulting from post-fabrication passivation of said interface in a heated, deuterium gas-enriched atmosphere at a temperature of about 200°C to about 1000°C so as to increase the resilience of the field effect transistor to hot electron effects, said post-fabrication passivation being conducted sufficiently to provide to said transistor a practical lifetime at least about ten times that provided by a corresponding passivation with hydrogen, wherein practical lifetime is taken as 20% transconductance degradation as a result of electrical stress.

41. (Amended) The semiconductor device of claim 40 wherein said gate ~~oxide~~ insulating layer comprises silicon dioxide.

48. (Twice Amended) The semiconductor device of claim 40, which comprises a drain formed in said semiconductive silicon layer, a source formed in said semiconductive silicon layer, a channel extending between the drain and the source, said gate ~~oxide~~ insulating layer over said channel, said interface between said gate insulating ~~oxide~~ layer and said channel, and conductive contacts for said drain, said source and said gate insulating~~oxide~~; and

wherein said post-fabrication passivation is carried out after formation of at least

said ~~conductive~~ gate contacts and produces a structure including covalently-bound deuterium populating said interface.

60. (Amended) The semiconductor device of claim 40, wherein said gate insulating~~oxide~~ layer comprises an oxide of silicon.

61. (Amended) The semiconductor device of claim 40, wherein said gate insulating~~oxide~~ layer comprises silicon dioxide or silicon oxy nitride.

62. (Amended) A semiconductor device comprising a field effect transistor having an interface between a semiconductive silicon layer and a gate insulating~~oxide~~ layer, a drain formed in said semiconductive silicon layer, a source formed in said semiconductive silicon layer, a channel extending between the drain and the source, said gate insulating~~oxide~~ layer over said channel, said interface between said gate insulating~~oxide~~ layer and said channel, and conductive contacts for said drain, said source and said gate insulating layer~~oxide~~; said semiconductive device structurally characterized by post-fabrication heating of the device after formation of at least said gate contacts, in a deuterium gas-enriched atmosphere at a temperature of about 200°C to about 1000°C to provide deuterium at and to passivate said interface so as to increase the resilience of the field effect transistor to hot electron effects.

63. (Amended) The semiconductor device of claim 62 wherein said gate insulating ~~oxide~~ layer comprises silicon dioxide.

67 (Amended) The device as recited in claim 66 wherein said film is ~~selected from the group consisting of:~~

a dielectric film, and said transistor gate comprises a polysilicon ~~film~~.

69 (Amended) The device as recited in claim 68 wherein said ~~polysilicon film~~transistor gate is comprised of polycrystalline silicon.

72. (Amended) The device as recited in claim 66 wherein said substrate is comprised of a material selected from the group consisting of:
a Group IV element ~~silicon, germanium,~~ and gallium arsenide.

79 (New). A semiconductor device comprising a field effect transistor having an interface between a semiconductive silicon layer and a gate insulating layer, structurally characterized by the gate insulating layer having a thickness not exceeding about 55 Angstroms and by the presence of deuterium at said interface resulting from post-fabrication passivation of said interface in a heated, deuterium gas-enriched atmosphere at a temperature of about 200°C to about 1000°C so as to increase the resilience of the field effect transistor to hot electron effects, said post-fabrication passivation being conducted sufficiently to provide to said transistor a practical lifetime at least about ten times that provided by a corresponding passivation with hydrogen, wherein practical lifetime is taken as 20% transconductance degradation as a result of electrical stress.

80.. (New) A semiconductor device comprising a field effect transistor having an interface between a semiconductive silicon layer and a gate insulating layer, a drain formed in said semiconductive silicon layer, a source formed in said semiconductive silicon layer, a channel extending between the drain and the source, said gate insulating layer over said channel, said interface between said gate insulating layer and said channel, and conductive contacts for said drain, said source and said gate insulating layer; said semiconductive device structurally characterized by said gate insulating layer having a thickness not exceeding about 55 Angstroms and by annealing of the device after formation of at least said gate contact, in a deuterium gas-enriched atmosphere at a temperature above about 200°C to provide deuterium at said interface between said gate insulating layer and said channel to passivate said interface so as to

increase the resilience of the field effect transistor to hot electron effects.

81. (New) An improved semiconductor device including an insulated gate field effect transistor device having a transistor gate and a gate insulator film not exceeding about 55 Angstroms thickness interposed between said transistor and a channel of said transistor device and a concentration of deuterium introduced into and remaining within said film, said transistor device susceptible to degradation associated with hot carrier stress, said concentration of deuterium substantially reducing said degradation associated with said hot carrier stress.